PENDING CLAIMS AS AMENDED

Cancel claims 1-7.

8. (Original) An address generation apparatus for an interleaver in a wireless communication system, the apparatus comprising:
a counter; and
a plurality of address generators each coupled to the counter, each of the plurality of address generators comprising:
a memory storage device coupled to the counter, storing a plurality of counter values with corresponding counter offset values; and
a second counter coupled to the memory storage device, adapted to add the counter offset value to a previously generated address.

9. (Original) The apparatus as in claim 8, wherein the second counter comprises:
an adder having a first input coupled to the memory storage device;
a multiplexor having a first input coupled to an output of the adder and a second input coupled to a predetermined initialization value; and
a second memory storage device coupled to the output of the multiplexor and having an output coupled to a second input to the adder.

10. (Original) The apparatus as in claim 9, further comprising:
append circuitry coupled between the memory storage device and the second counter, wherein the append circuitry appends a predetermined value to the output of the memory storage device.

11. (Original) The apparatus as in claim 10, wherein the first memory storage device is a look up table.

12. (Currently Amended) A data encoder, comprising:
a plurality of memories for storing sequential input information bits;
a plurality of interleavers for scrambling the input information bits, each of the plurality of interleavers configured to receive input information bits in ~~paralle~~ parallel;

a first encoder coupled to a first of the memories, the first encoder adapted to encode the sequential input information bits; and

a second encoder coupled to the plurality of memories, the second encoder adapted to encode the interleaved input information bits.

13. (Original) The data encoder as in claim 12, wherein the first encoder and the second encoder process multiple bits per system clock cycle.

14. (Original) The data encoder as in claim 13, wherein the first encoder and the second encoder include a plurality of AND-XOR trees.

15. (Original) The data encoder as in claim 14, wherein the first encoder and the second encoder recursively process multiple bits.

Cancel claim 16.

Claims 17-18. (Cancelled)

Cancel claims 19 – 27.